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Analog/RF Performance of T-Shape Gate Dual-Source Tunnel Field-Effect Transistor

Shupeng Chen, Hongxia Liu[*], Shulong Wang[*], Wei Li, Xing Wang and Lu Zhao

Abstract

In this paper, a silicon-based T-shape gate dual-source tunnel field-effect transistor (TGTFET) is proposed and investigated by TCAD simulation. As a contrastive study, the structure, characteristic, and analog/RF performance of TGTFET, LTFET, and UTFET are discussed. The gate overlap introduced by T-shape gate can enhance the efficiency of tunneling junction. The dual-source regions in TGTFET can increase the on-state current (I_{ON}) by offering a doubled tunneling junction area. In order to further improve the device performance, the n+ pocket is introduced in TGTFET to further increase the band-to-band tunneling rate. Simulation results reveal that the TGTFET's I_{ON} and switching ratio (I_{ON}/I_{OFF}) reach 81 μA/μm and 6.7×10^{10} at 1 V gate to source voltage (V_g). The average subthreshold swing of TGTFET (SS_{avg}, from 0 to 0.5 V V_g) reaches 51.5 mV/dec, and the minimum subthreshold swing of TGTFET (SS_{min}, at 0.1 V V_g) reaches 24.4 mV/dec. Moreover, it is found that TGTFET have strong robustness on drain-induced barrier lowering (DIBL) effect. The effects of doping concentration, geometric dimension, and applied voltage on device performance are investigated in order to create the TGTFET design guideline. Furthermore, the transconductance (g_m), output conductance (g_{ds}), gate to source capacitance (C_{gs}), gate to drain capacitance (C_{gd}), cut-off frequency (f_T), and gain bandwidth (GBW) of TGTFET reach 232 μS/μm, 214 μS/μm, 0.7 fF/μm, 3.7 fF/μm, 11.9 GHz, and 2.3 GHz at 0.5 V drain to source voltage (V_d), respectively. Benefiting from the structural advantage, TGTFET obtains better DC/AC characteristics compared to UTFET and LTFET. In conclusion, the considerable good performance makes TGTFET turn into a very attractive choice for the next generation of low-power and analog/RF applications.

Keywords: T-shaped gate, Recessed gate, Tunnel field-effect transistor (TFET), Analog/RF performance

Background

The scaling down of metal-oxide-semiconductor field-effect transistors (MOSFETs) brings significant improvement in integrated circuit (IC) power consumption, switching characteristic, circuit function, and IC density [1, 2]. But the irreconcilable contradiction between the scaling of the supply voltage and the reduction of the off-state leakage currents (I_{OFF}) will finally result in the unacceptable high power consumption [3]. At the same time, reliability degradation caused by short-channel effects (SCEs) becomes more and more serious [4, 5]. In order to address these problems, it is valid to reduce subthreshold swing (SS) and supply voltage of the devices. Based on the band-to-band tunneling mechanism, tunnel field-effect transistors (TFETs) reach the subthreshold swing (SS) smaller than 60 mV/dec and could effectively reduce the supply voltage [6–10]. Moreover, due to the existence of the tunneling junction near the source, TFET usually has a small gate to source capacitance (C_{gs}) [1, 11] which is beneficial to the device frequency performance.

Recent studies show that TFET seems to be a promising candidate for future low-power applications [12–16] and analog/RF applications [17–19]. However, due to the small effective tunneling area, the limited tunneling current becomes an inherent disadvantage in conventional P-I-N TFET, which leads to a low on-state operating current (I_{ON}). In order to improve the TFET performance, many new structures have been proposed in recent years [20–25]. Benefiting from the recessed gate, L-shape tunnel field-effect transistor (LTFET) [23, 24] and U-shape tunnel field-effect transistor (UTFET) [25] have been proposed to obtain high I_{ON} with a

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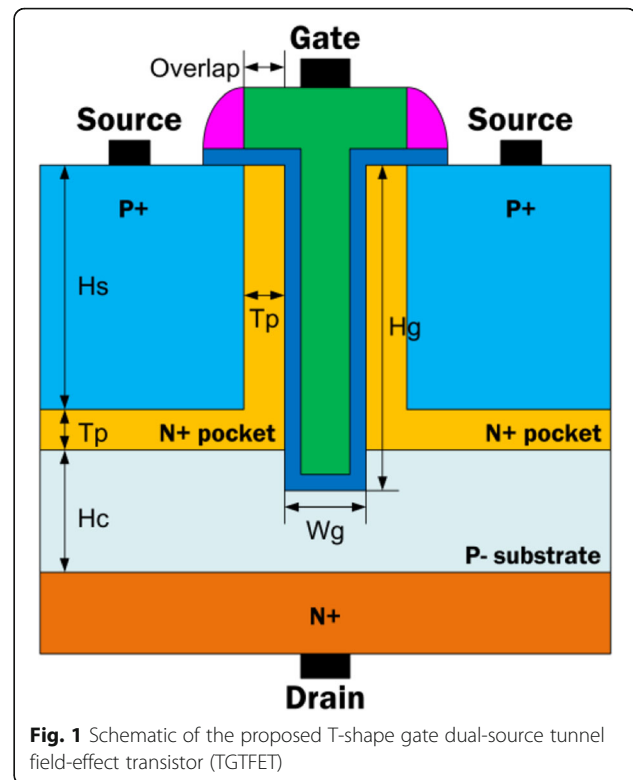Chen *et al. Nanoscale Research Letters* (2018) 13:321

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compact device structure. However, there is still much room for improvement in LTFET and UTFET and needs to spend more effort to study the analog/RF performance of these devices.

In this paper, a T-shape gate dual-source tunnel field-effect transistor (TGTFET) with dual source is put forward and studied by TCAD simulation. The designed TGTFET can double the tunneling junction area compared with LTFET and UTFET. The gate overlap introduced by the designed T-shape gate can enhance the band-to-band tunneling rate (BBT rate). The simulation results show that the proposed TGTFET gains a higher I_{ON} (8.1×10^{-5} A/μm at $V_d = 1$ V) than the LTFET and UTFET under the same condition. Both of the SS_{min} (at $V_g = 0.1$ V) and the SS_{avg} (0~0.5 V V_g) of TGTFET are lower than 60 mV/dec (24.4 mV/dec and 51.5 mV/dec, respectively). TGTFET gains better input/output characteristic ($g_m = 232$ μS/μm, $g_{ds} = 214$ μS/μm) than the UTFET and LTFET. Moreover, the capacitance characteristics of TGTFET, UTFET, and LTFET are discussed in detail. Finally, TGTFET gains better analog/RF performance ($f_T = 11.9$ GHz and GBW = 2.3 GHz) compared to UTFET and LTFET. As a result, TGTFET with considerable good performance can be obtained. The structures of this paper are as follows: the "Methods" section includes the description of the structure and the parameters of TGTFET, LTFET [23, 24], and UTFET [25] as well as the TCAD simulation methods. The "Results and Discussion" section includes the description of the simulation results. In this section, the mechanism, characteristic, and analog/RF performance of TGTFET are studied and compared with the LTFET and UTFET. The influence of the device parameters on TGTFET is analyzed in detail too. The "Conclusions" section gives a conclusion of this paper.

Methods

The structure of T-shape gate dual-source tunnel field-effect transistor (TGTFET) is illustrated in Fig. 1. The shape of the gate is similar to the alphabet letter "T" (green region). The dual-source regions are located on two sides of the gate (sapphire regions). Two n+ pockets (yellow regions) are inserted to increase the channel tunneling rate [20–22]. The n+ drain is placed in the bottom of the channel. Therefore, the T-shaped gate overlaps the n+ pockets in both the vertical and lateral directions. By this way, the electric field at the top of the tunneling junction can be increased. The electric field enhancement causes the energy band to bend more steeply. Finally, the electron tunneling rate is enhanced due to the corner electric field enhancement [26].
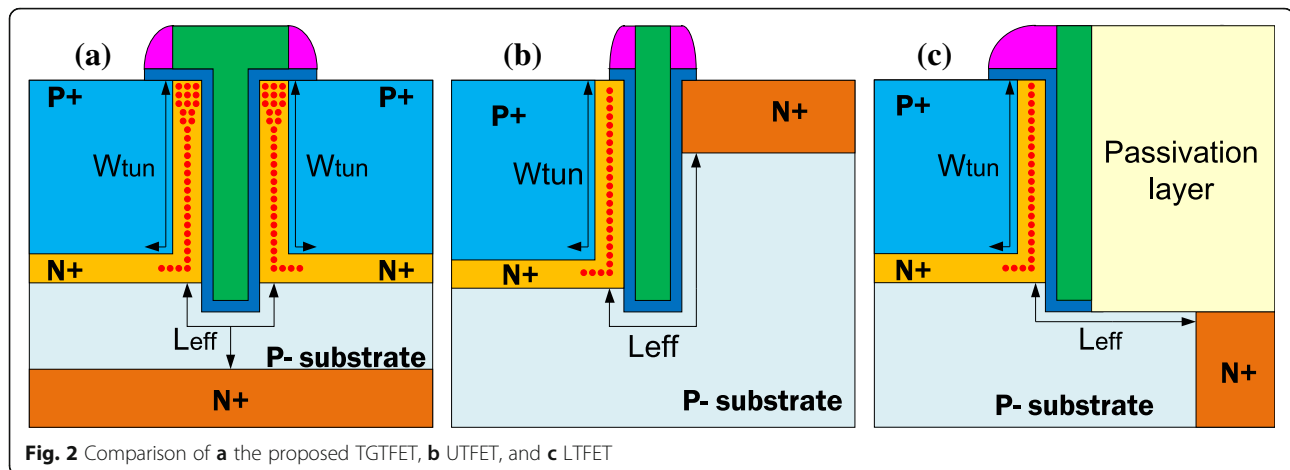
Figure 2 shows the device structure of LTFET [23, 24], UTFET [25], and TGTFET. The gate overlap can help to enhance the tunneling efficiency of TGTFET. The

Fig. 1 Schematic of the proposed T-shape gate dual-source tunnel field-effect transistor (TGTFET)

dual-source regions in TGTFET can double the tunneling junction area compared with LTFET and UTFET.

Parameters of silicon-based TGTFET, UTFET, and LTFET used in simulations are as follows: Hs = 30 nm (height of the source region), Hg = 40 nm (height of the recessed gate), Wg = 6 nm (width of the gate region), Hc = 15 nm (height of the channel region), Tp = 5 nm (thickness of the n+ pocket), $\phi = 4.33$ eV (gate work function), Tox = 2 nm (thickness of the HfO$_2$ gate dielectric), $N_S = 1 \times 10^{20}$ cm^{-3} (p+ source doping concentration), $N_D = 1 \times 10^{19}$ cm^{-3} (n+ drain doping concentration), $N_{sub} = 1 \times 10^{17}$ cm^{-3} (p– substrate doping concentration), and $N_P = 5 \times 10^{18}$ cm^{-3} (n+ pocket doping concentration). The width coefficient in simulation is default to 1 μm.

Simulations of TGTFET, UTFET, and LTFET are carried out in Silvaco Atlas TCAD tools. Non-local BTBT model is introduced in this simulation to bring the energy band spatial variation into account, which can help to facilitate the accuracy of the BTBT tunneling process. Lombardi mobility model is considered to make the channel mobility more accurate (by considering the surface scattering including the transverse field and doping concentration). Fermi statistics and band gap narrowing model is taken into account to fit the effect of the highly doped regions. Shockley-Read-Hall recombination model is taken into account in this paper, too.

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Fig. 2 Comparison of **a** the proposed TGTFET, **b** UTFET, and **c** LTFET

Results and Discussion

Device Mechanism and DC Characteristics with Different Parameters
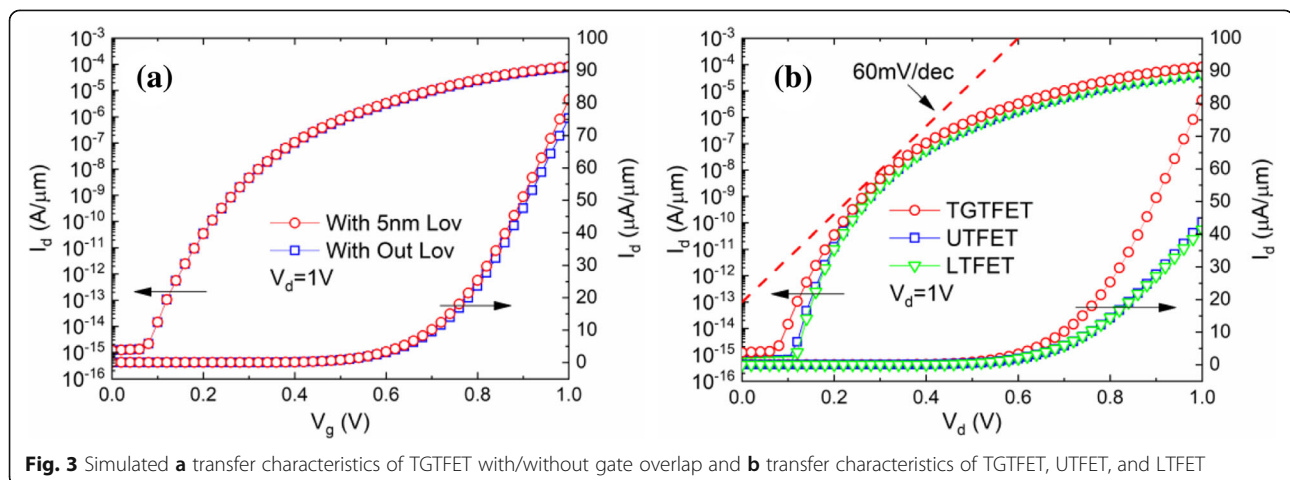
Figure 3a shows the transfer characteristics of the TGTFET with and without the gate overlap. With the additional gate overlap, the I_{ON} increases from 7.5×10^{-5} to 8.1×10^{-5} A/μm at $V_g = V_d = 1$ V. Figure 3b shows the transfer characteristic curves of TGTFET, UTFET, and LTFET. In order to make the comparison more accurate, the simulation models and geometric dimensions of these three devices are set to be identical. As a result, the TGTFET has about a twofold increase in I_{ON} compared with LTFET and UTFET, as shown in Fig. 3b. SS_{min} of TGTFET is 24.4 mV/dec at $V_g = 0.1$ V, and SS_{avg} is 51.5 mV/dec when $0\ V < V_g < 0.5$ V. The switching ratios (I_{ON}/I_{OFF}) are 6.7×10^{10} at $V_g = V_d = 1$ V and 6.5×10^8 at $V_g = V_d = 0.5$ V.
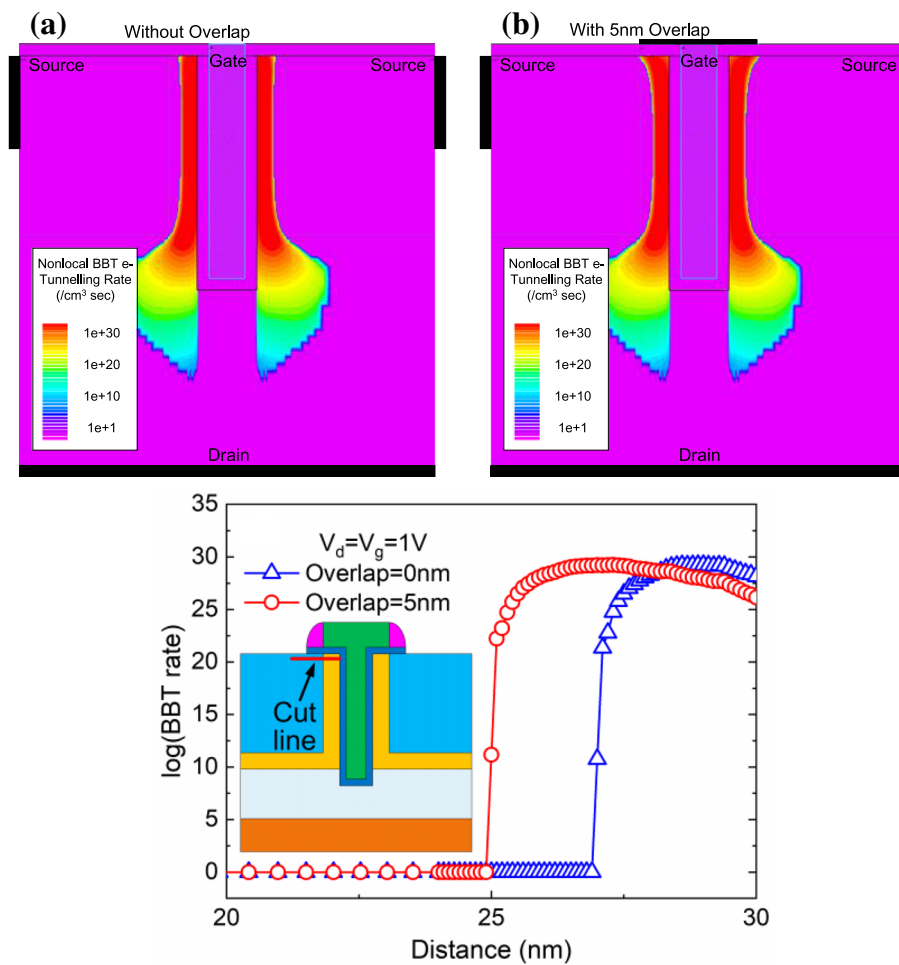
Figure 4a, b shows the BBT rate of TGTFET with and without a 5-nm gate overlap. From Fig. 4c, we can clearly see that the device with a 5-nm gate overlap has a wider electron tunneling area under the device surface, which can lead to the I_{ON} increasing.

Figure 5a, b shows the 3D diagram of electric fields of TGTFET with and without gate overlap. Two electric field peaks appear in TGTFET with a 5-nm gate overlap, as shown in the dashed circle in Fig. 5a. No electric field peak appears in Fig. 5b attributed to the absences of the gate overlap. Figure 5c shows the energy band structure under the surface of the device. The inset in Fig. 5c shows the cut line location. With the gate overlap, a larger tunneling window can be obtained. Thus, a higher BBT rate and I_{ON} can be achieved.

Figure 6 shows the effects of n+ pocket on the performance of the TGTFET. The I_{OFF} increases rapidly with the increasing of the n+ pocket doping concentration, as shown in Fig. 6a. The lower SS and greater I_{ON} can be obtained by decreasing the thickness of n+ pocket (Tp) from 7 to 3 nm when $N_P = 5 \times 10^{18}$ cm^{-3}, as shown in Fig. 6b. At the same time, no significant subthreshold current is noted in Fig. 6b. It can be confirmed from Fig. 6a that a relatively low doping concentration of n+ pocket will help to suppress the subthreshold current.

The impact of the gate height (Hg) and channel thickness (Hc) is shown in Fig. 7a, b, separately. A small I_{ON}

Fig. 3 Simulated **a** transfer characteristics of TGTFET with/without gate overlap and **b** transfer characteristics of TGTFET, UTFET, and LTFET

Fig. 4 Simulated BBT electron tunneling rate diagrams of **a** device without gate overlap, **b** device with 5-nm gate overlap, and **c** the BBT electron tunneling rate of two devices, at 1 nm below the device surface; $V_g = V_d = 1$ V

and SS improvement appears when Hg is increasing. Because when Hg = 35 nm, there is an obvious energy band hump on the on-state current path, becoming a certain obstacle to the lucky electrons (electrons which passed the tunneling junction), as shown in Fig. 7c, which can result in I_{on} decrease. When Hg increases, the energy band hump is weakened, which cause the I_{ON} and SS improvement. A slight I_{ON} improvement is obtained with Hc decreasing, as shown in Fig. 7b. However, severe degradation on subthreshold characteristic can be observed when Hc decreases to 5 nm. This can be explained by the increasing subthreshold tunneling current at the corner of the n+ pocket, as shown in Fig. 8. Figure 8a shows the obvious off-state band-to-band tunneling phenomenon when Hc = 5 nm while Fig. 8b shows the I_{OFF} current density when Hc = 5 nm.

As shown in Fig. 9, the influence of drain to source voltage (V_d) is also taken into account in this paper. For $V_d <$ 0.6 V, I_{ON} increases obviously with the increasing V_d, as

shown in Fig. 9a. This is explained by the fact that the potential of the p-channel is slowly growing in response to the increasing V_d and results in the decreasing resistance of p-channel. For $V_d > 1.8$ V, shown in Fig. 9b, the I_{ON} almost does not increase with the increasing V_d, but I_{OFF} increases considerably. This is because of the subthreshold tunneling current at the corner of the n+ pocket increasing rapidly with the increasing V_d. Finally, for 0.6 V $< V_d <$ 1.8 V, TGTFET exhibits good and stable performance. As a result, TGTFET is robust to drain-induced barrier lowering (DIBL) and exhibits a good and stable performance in a larger applied voltage dynamic range.

Analog/RF Performance of TGTFET, UTFET, and LTFET

Figure 10 shows the transfer characteristics and transconductance curves of TGTFET, UTFET, and LTFET at $V_d = 0.5$ V. The transconductance (g_m) can be obtained from the first derivative of the transfer characteristic curve, as shown in Eq. (1) [27–29]:
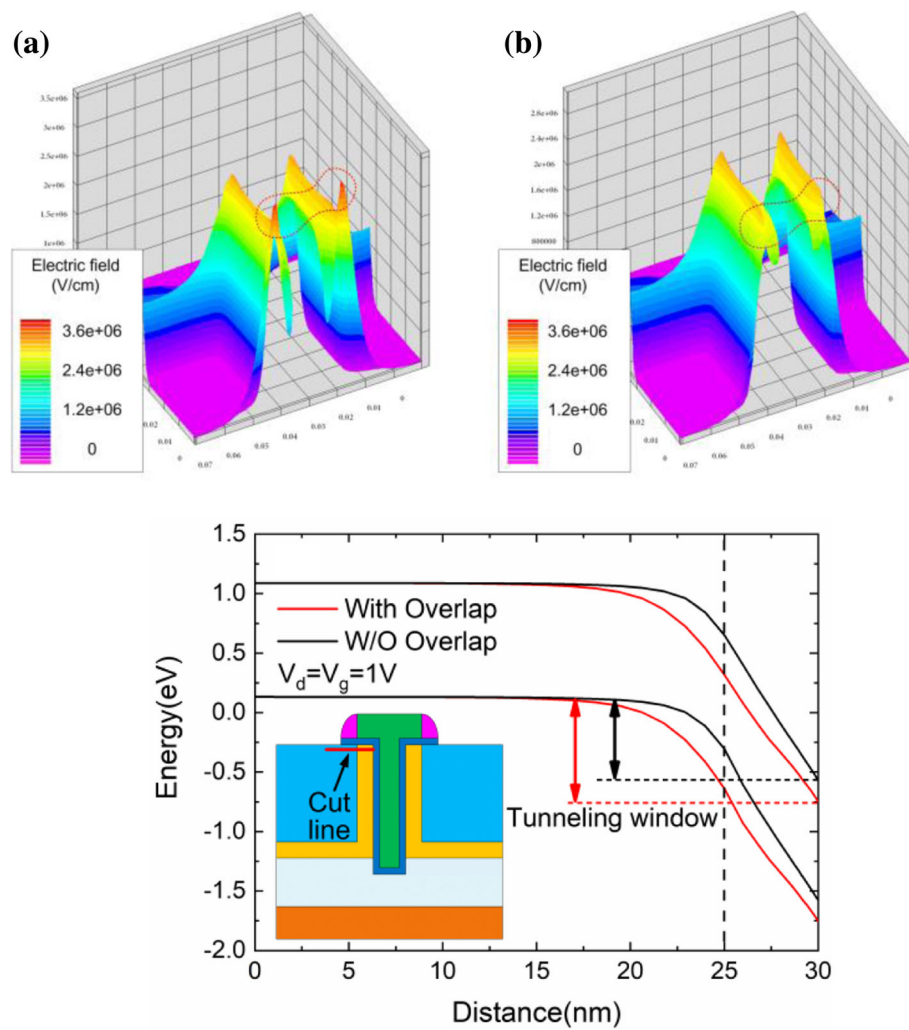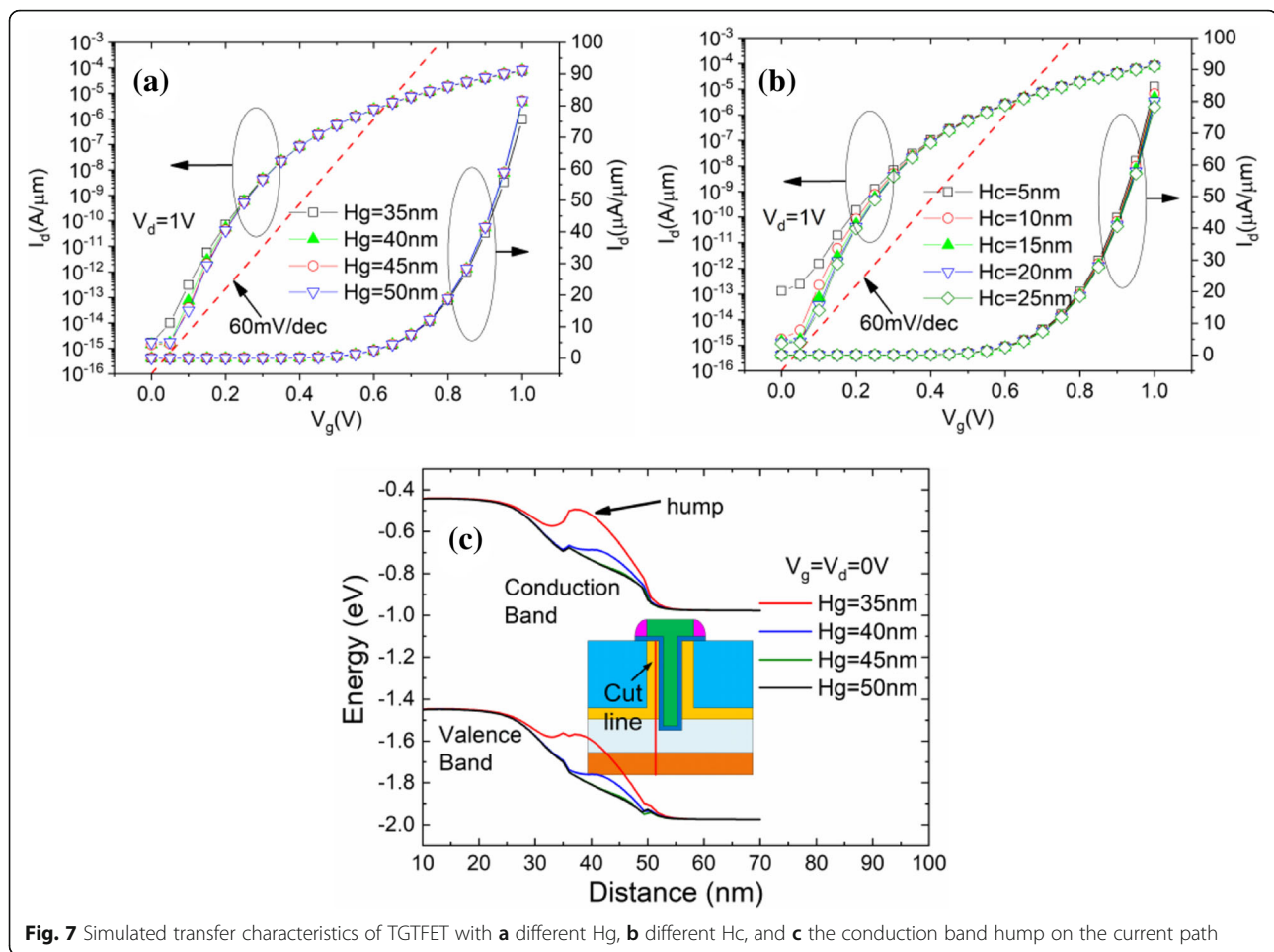
Fig. 5 3D schematic diagram of electric fields of the device **a** with overlap and **b** without overlap; simulated **c** energy band diagrams from source to pocket region (1 nm below the oxide interface)
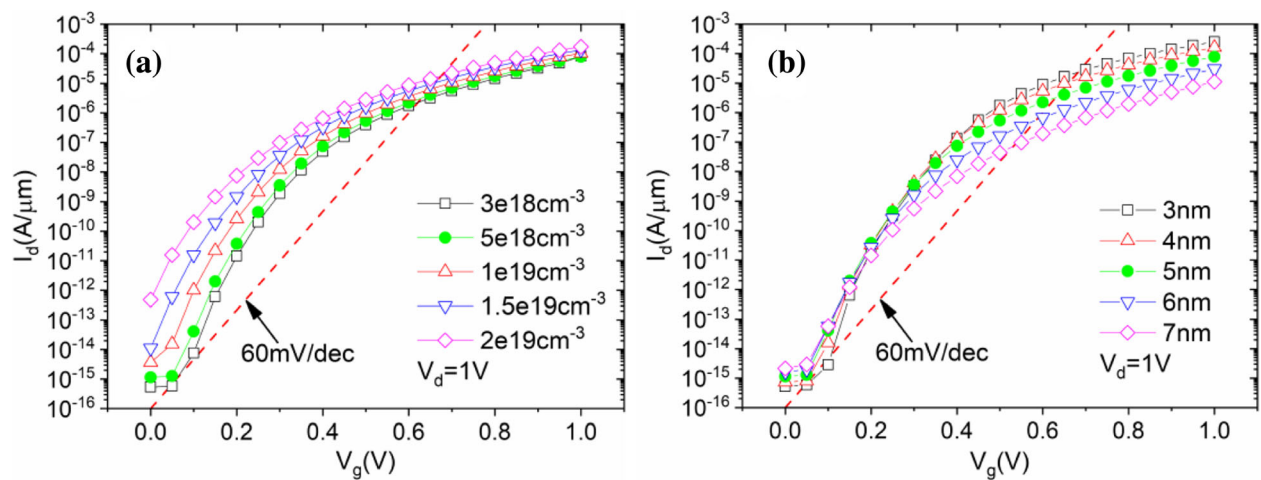
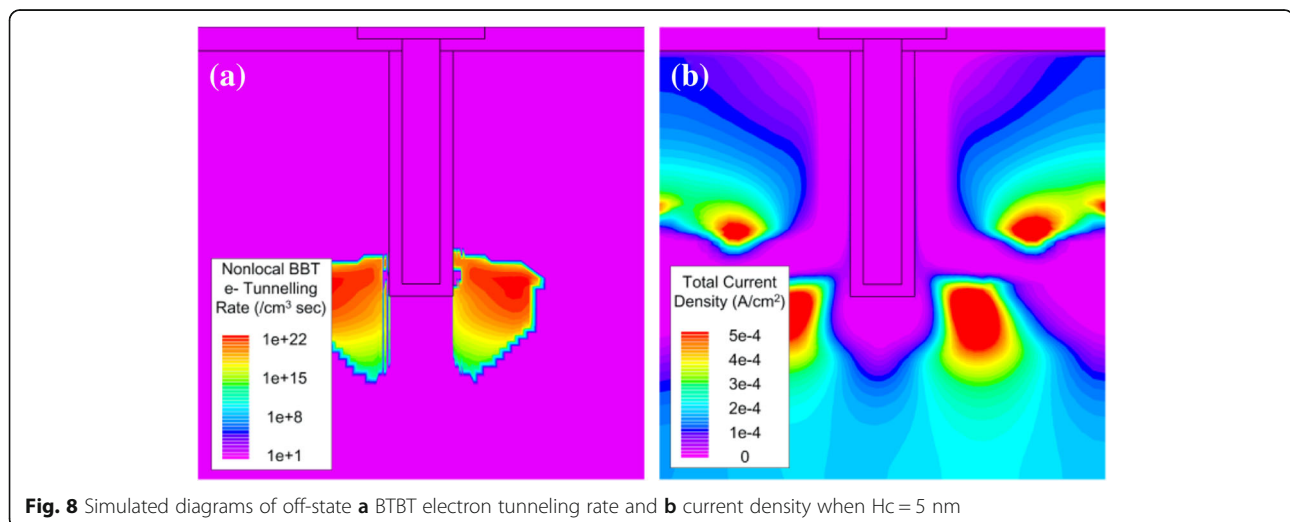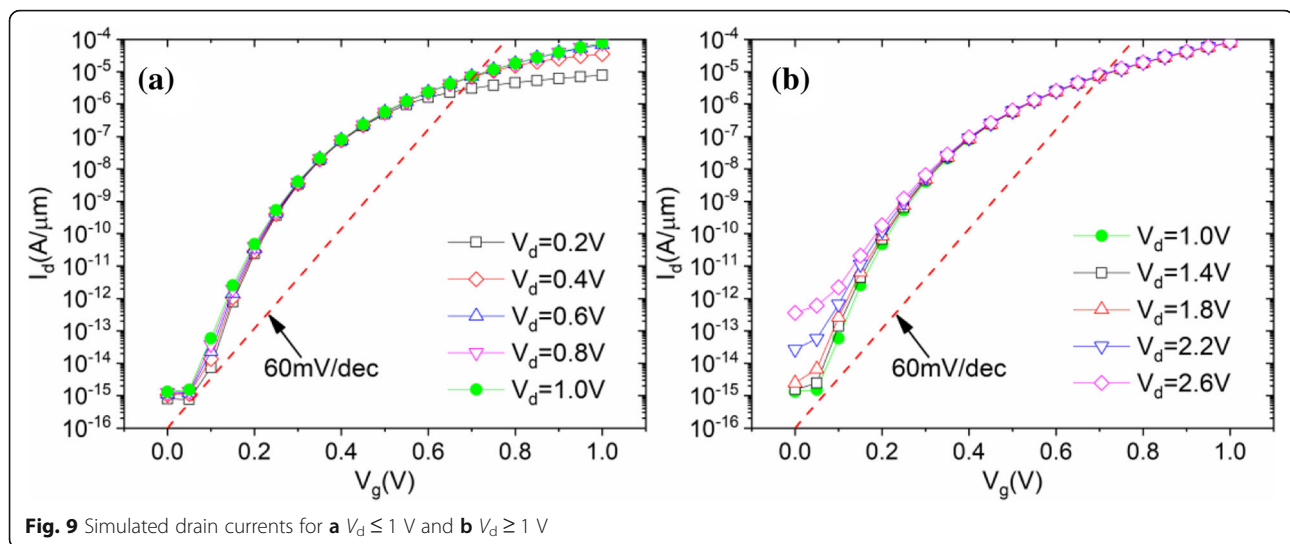**Fig. 6** Simulated drain currents with different n+ pocket **a** concentrations and **b** thicknesses at $V_d = 1$ V

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Fig. 7 Simulated transfer characteristics of TGTFET with **a** different Hg, **b** different Hc, and **c** the conduction band hump on the current path

$$g_m = dI_{ds}/dV_{gs} \qquad (1)$$

As a result, the maximum transconductance of TGTFET (232 μS/μm) is about two times larger than that of UTFET (120 μS/μm) and LTFET (110 μS/μm), as

shown in Fig. 10. This is benefited from the current gain contributed by dual source and gate overlap.

Figure 11 shows the output characteristics, output conductance (g_{ds}), and output impedance (R_o) curves of the TGTFET, UTFET, and LTFET. As shown in Fig. 11a,

Fig. 8 Simulated diagrams of off-state **a** BTBT electron tunneling rate and **b** current density when Hc = 5 nm

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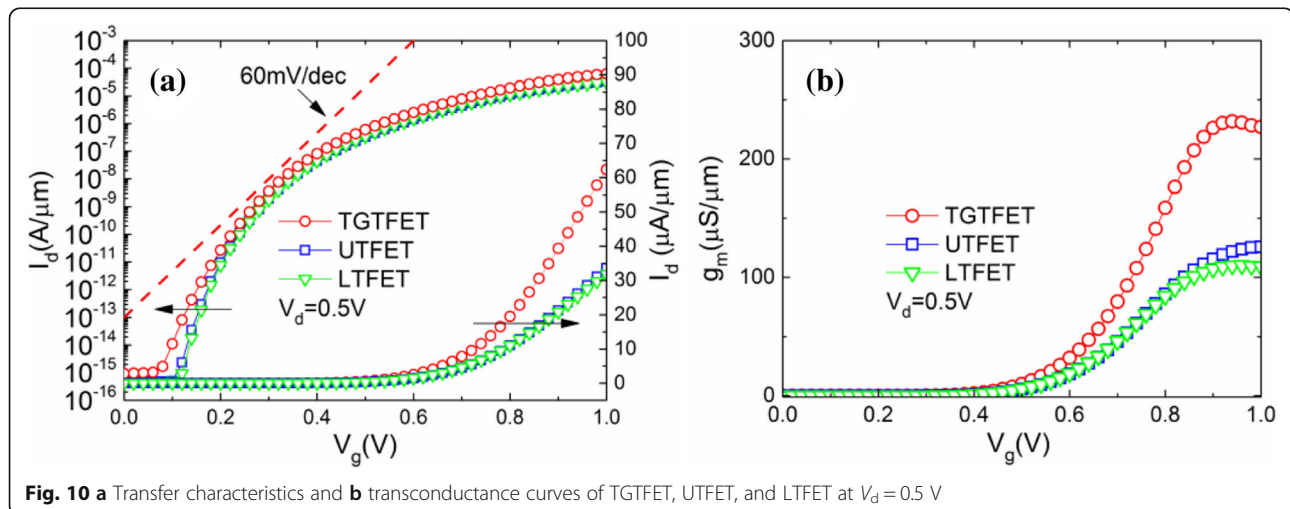**Fig. 9** Simulated drain currents for **a** $V_d \leq 1$ V and **b** $V_d \geq 1$ V

it can be clearly seen that the output current of the device increases with the increase of V_d, but when V_d reaches above 0.6 V, the output current tends to saturate. Through observation, it is easy to find that the output current of TGTFET is two times larger than that of UTFET and LTFET. Figure 11b shows the output conductance (g_{ds}) and output impedance (R_o) curves of the TGTFET, UTFET, and LTFET. The g_{ds} can be obtained through the derivation of the output current, as shown in Eq. (2) [27, 29] while R_o can be expressed as the reciprocal of the output conductance.
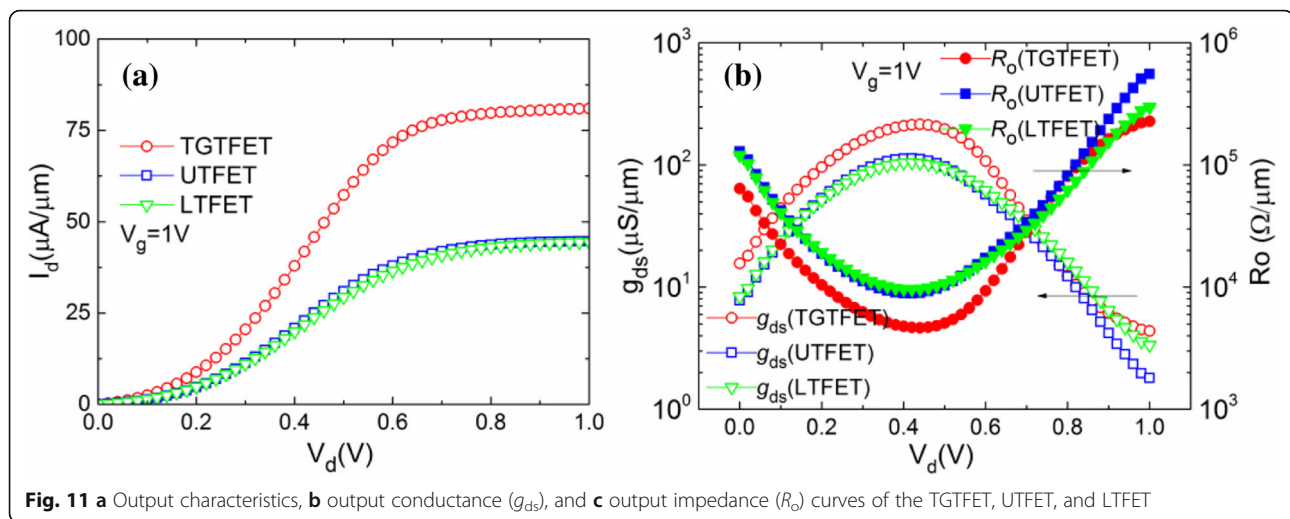
$$g_{ds} = dI_{ds}/dV_{ds} \qquad (2)$$

Due to the advantages on output current, TGTFET gains the highest g_{ds} and the minimum R_o of these three devices. Under 1-V gate bias condition, TGTFET obtained the maximum g_{ds} of 214 μS/μm and the minimum R_o of

4.6 kΩ/μm under 0.45 V V_d. Under the same gate bias condition, UTFET and LTFET obtained the maximum g_{ds} of 113 μS/μm and 105 μS/μm and the minimum R_o of 9.0 kΩ/μm and 9.6 kΩ/μm under 0.4 V V_d.

Moreover, in Fig. 11, it is not difficult to find out that the linear region of the device output characteristics shows certain nonlinearity. As shown in Fig. 11a, R_o decreases first and then increases with the increasing V_d. Some research groups give the corresponding physical process about this phenomenon [7, 30] but there are still some problems that have not been explained clearly. As we know, R_o is determined by the resistance of channel region and tunneling junction. When $V_d < 0.4$ V, R_o decreases with the increasing V_d. Consider the following situations, when $V_d = 0$ V and $V_g = 1$ V, none of the lucky electrons can be swept to the drain side, and almost all the electrons are trapped in the channel region by a relatively high drain barrier, as shown in the red dotted line frame in Fig. 12a, b. When 0 V < V_d < 0.4 V, with the

Fig. 10 a Transfer characteristics and **b** transconductance curves of TGTFET, UTFET, and LTFET at $V_d = 0.5$ V

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Fig. 11 a Output characteristics, **b** output conductance (g_{ds}), and **c** output impedance (R_o) curves of the TGTFET, UTFET, and LTFET
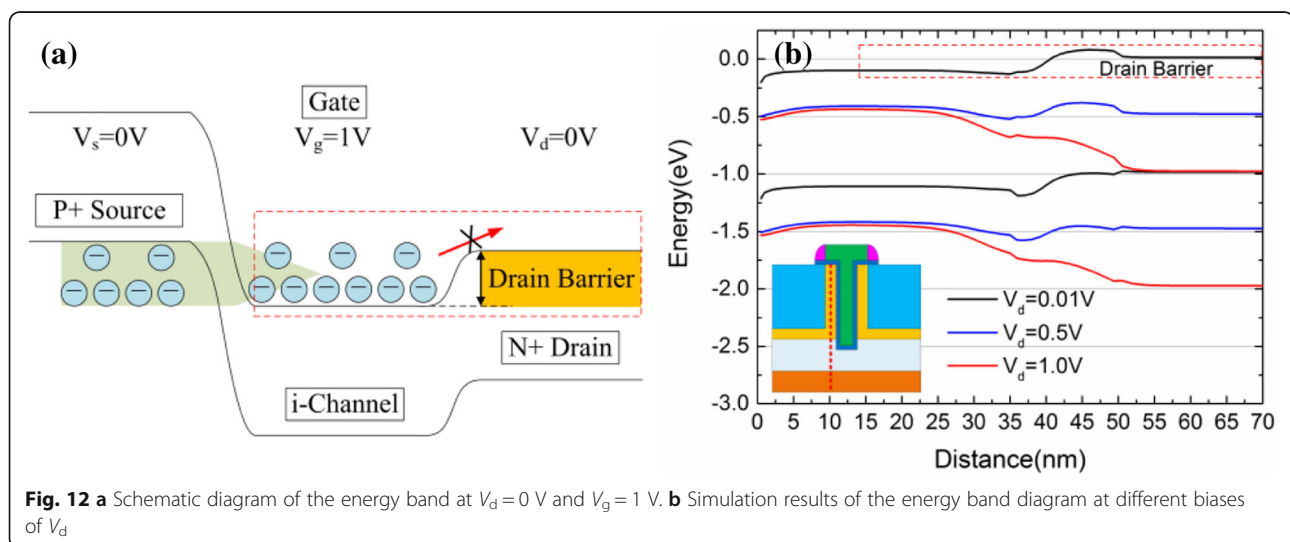
increasing of V_d, the drain barrier becomes weaker (as shown in Fig. 12b). Thus, the electrons trapped in the channel region can pass through the drain barrier and then be collected by drain. This is a thermal excitation process of electrons from channel to drain. Finally, as the tunneling junction has been completely turned on (when $V_g = 1$ V), the tunneling current is always in a state of excess and the resistance introduced by tunneling junction can be ignored. At this time, R_o is determined by the channel resistance and R_o is decided by the electron thermal excitation process across the drain barrier. Thus, R_o decreases with the increasing of V_d. When $V_d > 0.6$ V, these three devices gradually enter the saturation area and R_o becomes larger. This is because when V_d is large, almost all the electrons through the tunneling junction are swept to the drain side by the relatively high electric field. The tunneling current becomes the limit of the drain current. In this condition,

R_o is mainly determined by the tunneling junction. However, the tunneling efficiency cannot increase significantly while V_d is increasing. V_d has a small effect on the energy band structure of the tunneling junction (n+ pocket side), as shown in Fig. 12b. As a result, the tunneling current cannot increase obviously, and there is almost no I_{ON} increase with the continually increasing V_d (when $V_d > 0.6$ V), which means an impedance increases. Moreover, when 0.4 V $< V_d < 0.6$ V, R_o is determined by both the channel resistance and tunneling junction.

It can be obtained from the above analysis that the R_o of TFET is influenced by both the tunneling process and the channel electron thermal excitation process. The main physical mechanisms can dominate R_o shifts with V_d variation. Finally, the R_o decreases first and then increases, thus causing the nonlinearity of the output characteristics. Incidentally, through the observation of Fig. 11b, it is easy to find that the output impedance of

Fig. 12 a Schematic diagram of the energy band at $V_d = 0$ V and $V_g = 1$ V. **b** Simulation results of the energy band diagram at different biases of V_d

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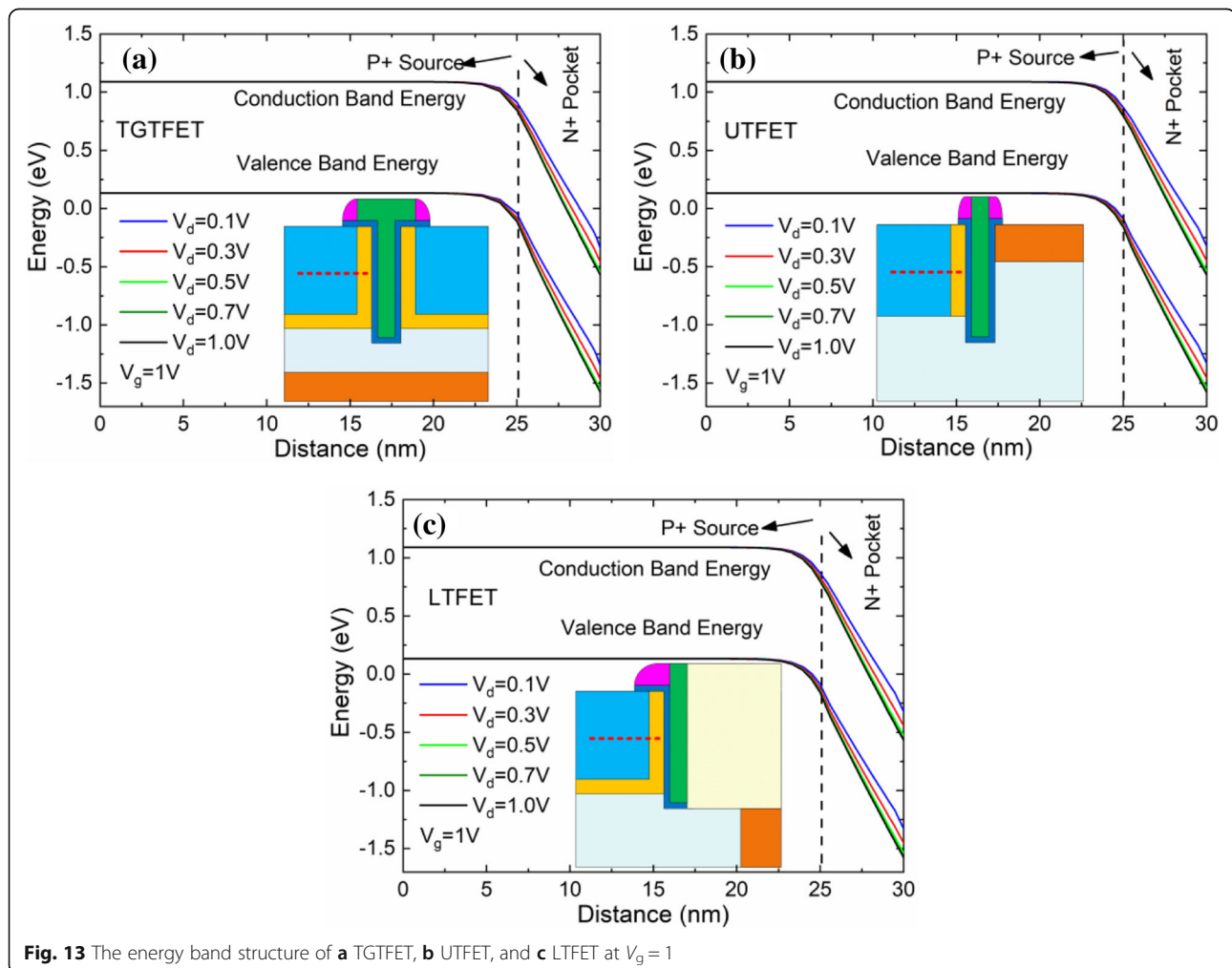
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TGTFET is much smaller than that of the UTFET and LTFET. This is due to the better tunneling efficiency benefit from the dual-source and the lateral gate overlap structure of TGTFET.
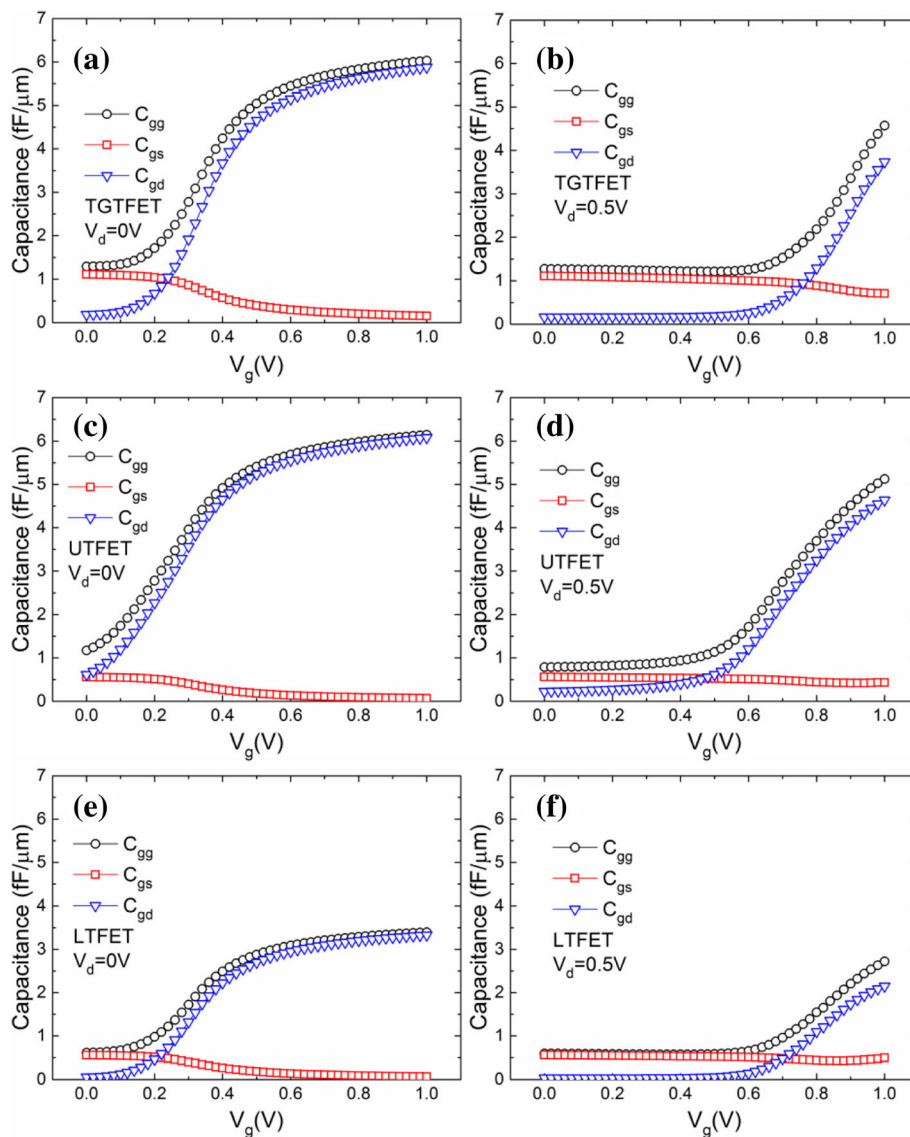
Figure 13 shows the energy band structure of TGTFET, UTFET, and LTFET with different applied voltages. The red dotted lines in the inset represent the position to draw the energy band (which is 15 nm below the surface, just at the 1/2 height of the source region). It can be seen that with a V_d increase from 0.1 to 0.5 V, the band structure of TGTFET, UTFET, and LTFET has an obvious trend of bending. This is because the drain voltage can pull down the electric potential of the tunneling junction near the drain side. This indicates that, for TGTFET, UTFET, and LTFET, the increase of V_d from 0.1 to 0.5 V is beneficial to tunneling efficiency. However, when $V_d >$ 0.5 V, the change of the energy band with V_d increase is not worth mentioning. This is consistent with the analysis results in Fig. 12b.

As we know, the gate capacitance (C_{gg}) of the device can greatly affect the frequency characteristics of the integrated circuits. For TGTFET, UTFET, and LTFET, C_{gg} generally consists of C_{gs} (capacitance of gate to source) and C_{gd} (gate to drain capacitance). Therefore, the characteristic of C_{gg}, C_{gs}, and C_{gd} is of great significance to evaluate the frequency characteristics and analog application ability of devices. Especially for TFET, the capacitance characteristics are quite different from MOSFET. Because of the existence of the tunneling junction at the source area, TFET usually has a small C_{gs} [1, 11]. Therefore, the C_{gg} of TFET is mainly determined by C_{gd}. Figure 14 shows the capacitance of TGTFET, UTFET, and LTFET versus V_g under $V_d =$ 0.5 V and $V_d = 0$ V, separately.

Through the observation of Fig. 14a, b, it is easy to find that the C_{gs} of TGTFET under 1-V gate voltage is 0.15 fF/μm at $V_d = 0$ V and 0.7 fF/μm at $V_d = 0.5$ V, which is far more smaller than that of the C_{gd} (5.8 fF/μm at $V_d = 0$ V and 3.7 fF/μm at $V_d = 0.5$ V). Thus, the C_{gg} of TGTFET is mainly determined by C_{gd}. When V_d = 0 V, C_{gg} and C_{gd} increase rapidly with the increasing V_g, as shown in Fig. 14a. This is because with the

Fig. 13 The energy band structure of **a** TGTFET, **b** UTFET, and **c** LTFET at $V_g = 1$

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Fig. 14 Capacitance of TGTFET versus V_g under **a** $V_d = 0$ V and **b** $V_d = 0.5$ V. Capacitance of UTFET versus V_g under **c** $V_d = 0$ V and **d** $V_d = 0.5$ V. Capacitance of LTFET versus V_g under **e** $V_d = 0$ V and **f** $V_d = 0.5$ V

increase of V_g, electrons are aggregated to the gate interface in the device channel, which makes the capacitance rise rapidly. When $V_d = 0.5$ V, C_{gd} does not increase obviously until V_g is increased to more than 0.6 V, as shown in Fig. 14b. This is because when V_g is low, only few lucky electrons can pass through the tunneling junction and go into the channel. Some of these lucky electrons will be participating in the recombination process, and most of the others will be rapidly collected by drain due to the 0.5-V drain voltage. Therefore, it is very difficult for these lucky electrons to stay in the device channel. However, with the V_g increase, the number of lucky electrons increases rapidly. At this moment, neither of the drain collection nor of the electron-hole recombination process

can rapidly deplete these lucky electrons. Thus, the electron concentration in the channel increases and the capacitance rises rapidly. As a result, the capacitance characteristic curve tends to shift right while V_d increases, as shown in Fig. 14a, b. The above analysis and phenomena are also applicable to UTFET and LTFET, as shown in Fig. 14c–f. In addition, the gate capacitance of UTFET at 0 V and 0.5 V V_d reached 6.2 fF/μm and 5.1 fF/μm, respectively, and that of the LTFET reached 3.4 fF/μm and 2.7 fF/μm, respectively.

Since there is no direct overlap between the LTFET's gate and drain, and the distance between the gate and drain is relatively far, LTFET has the best capacitance characteristics and the smallest C_{gg}. In contrast, there is

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a direct overlap between the UTFET's gate and drain. Therefore, electrons near the drain side are more easily controlled by gate, thus resulting in a large C_{gg} of UTFET. For TGTFET, although the distance between the gate and drain is close, but there is a lightly doped channel region which can isolate the gate and drain. Thus, the capacitance of TGTFET is better than that of the UTFET, but slightly inferior to LTFET. Figure 15 shows the C_{gd} characteristics of TGTFET, UTFET, and LTFET versus V_d under different V_g. From the observation of Fig. 15a–v, it is not difficult to find that the C_{gd} characteristics of these three devices are similar. That is, for a fixed V_g, C_{gd} decreases with the increase of the V_d. On the other hand, for a fixed V_d, C_{gd} increases with the increase of V_g.

As we know, both of the cut-off frequency (f_T) and gain bandwidth (GBW) are the evaluation criteria for evaluating th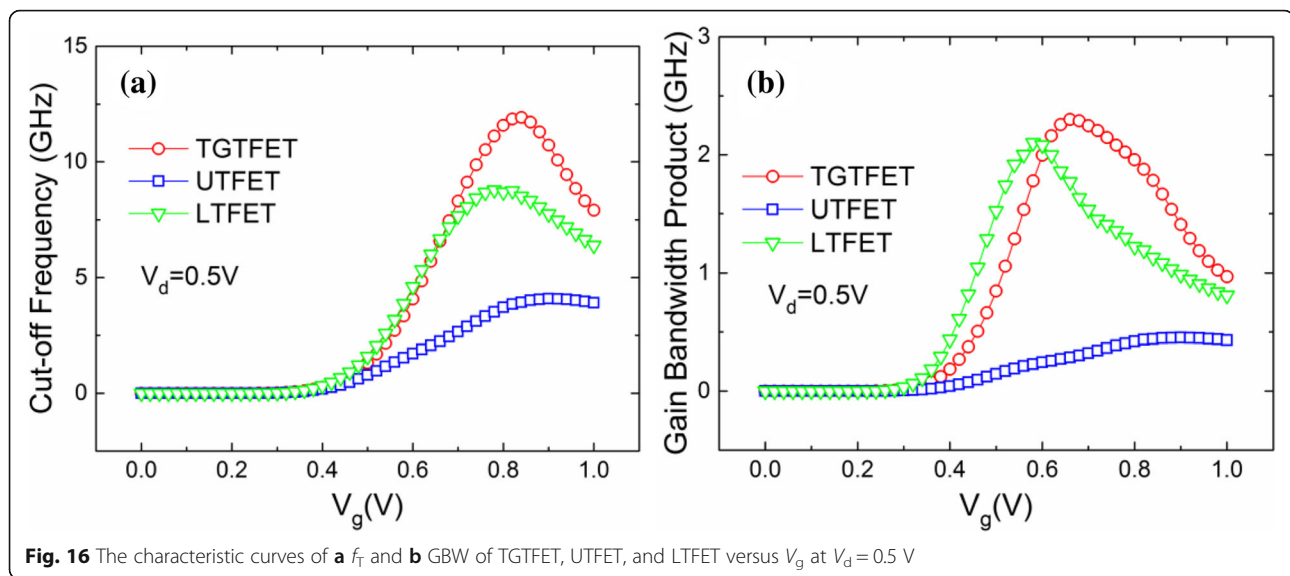e frequency characteristics of devices. f_T depends on the ratio of g_m to C_{gg}, as shown in Eq. (3) [30, 31]. For a certain DC gain that equals 10, GBW can be expressed by the ratio of g_m to C_{gd}, as shown in Eq. (4) [17]:

$$f_T = \frac{g_m}{2\pi C_{gs}\sqrt{1 + 2C_{gd}/C_{gs}}} \approx \frac{g_m}{2\pi(C_{gs} + C_{gd})} = \frac{g_m}{2\pi C_{gg}} \quad (3)$$

$$\text{GWB} = g_m/2\pi 10 C_{gd} \quad (4)$$

Figure 16 shows the characteristic curves of the f_T and GBW of TGTFET, UTFET, and LTFET. Benefiting from structural advantages, such as dual-source and lateral gate overlap introduced by the T-shaped gate, TGTFET obtains the most outstanding frequency characteristics compared with UTFET and LTFET. Under the condition of $V_d = 0.5$ V, the f_T and GBW of TGTFET reached the maximum values of 11.9 GHz and 2.3 GHz, respectively. Benefiting from the long distance between gate and drain and without gate/drain overlap, LTFET obtains a

Fig. 15 C_{gd} characteristics of **a** TGTFET, **b** UTFET, and **c** LTFET versus V_d under different V_g
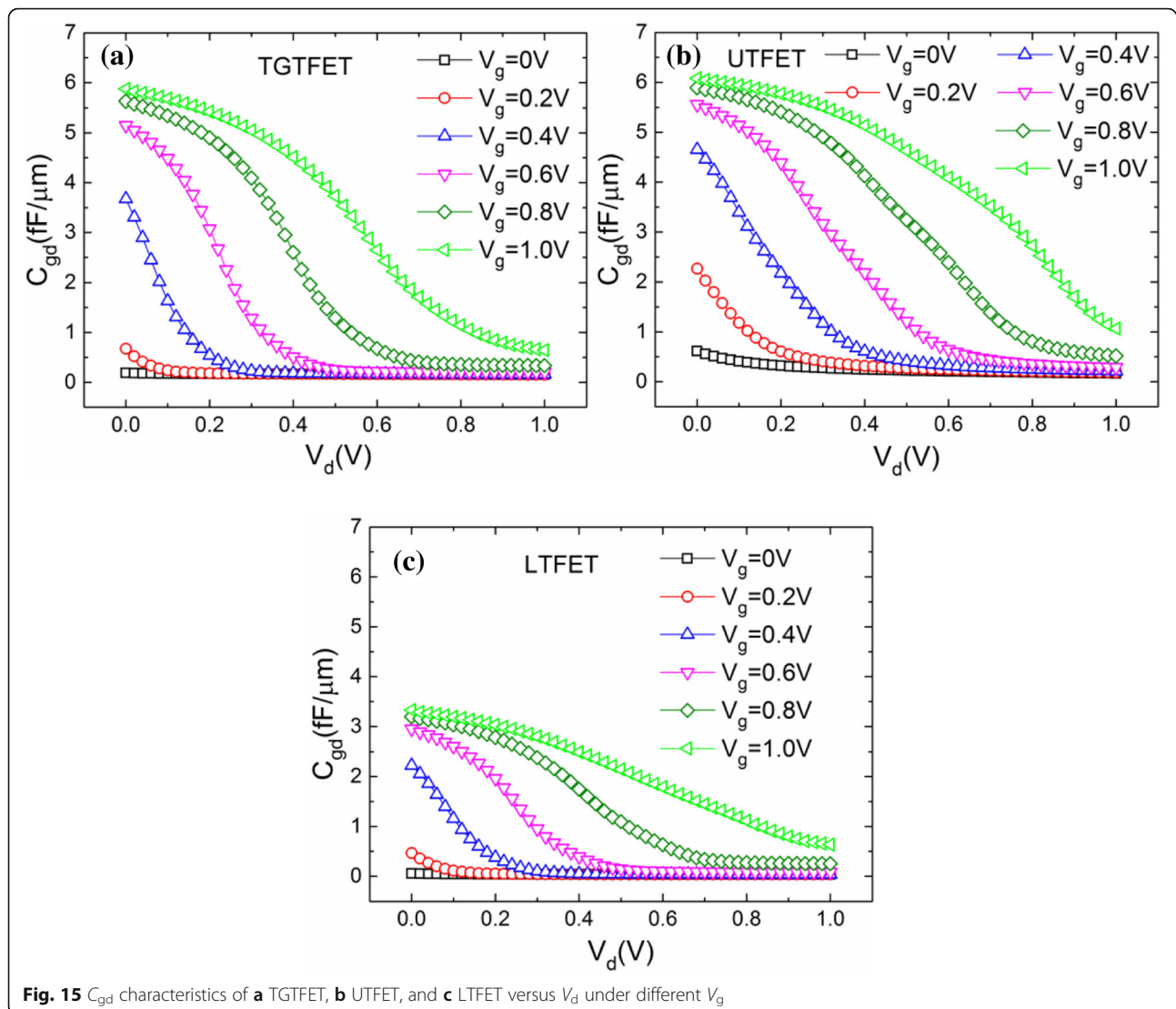
Fig. 16 The characteristic curves of **a** f_T and **b** GBW of TGTFET, UTFET, and LTFET versus V_g at $V_d = 0.5$ V

small C_{gg} and good frequency characteristics. The f_T and GBW of LTFET reach the 8.7 GHz and 2.1 GHz, separately. The capacitance characteristics of UTFET are inferior compared with that of TGTFET and LTFET. This is because the direct gate/drain overlaps. As a result, the maximum value of f_T and GBW of UTFET can only reach 4.1 GHz and 0.5 GHz separately.

Conclusions

In this paper, a T-shape gate dual-source tunnel field-effect transistor (TGTFET) with good performance is proposed and investigated. The structure, mechanism, and the influence of device parameter on the characteristic of TGTFET are discussed. In addition, the characteristics of TGTFET, UTFET, and LTFET are discussed and compared in this paper. The dual-source regions are introduced to double the area of the tunneling junction. The gate overlap and the n+ pockets can obviously enhance the tunneling efficiency of the tunneling junction in TGTFET. Finally, the TGTFET with impressive characteristics ($I_{ON} = 8.1 \times 10^{-5}$ A/μm, $I_{ON}/I_{OFF} = 6.7 \times 10^{10}$ and $SS_{min} = 24.4$ mV/dec) is obtained. At the same time, TGTFET is robust to DIBL, which means TGTFET can exhibit a good and stable performance in a larger applied voltage dynamic range. Furthermore, the analog/RF performance of TGTFET is studied and compared with UTFET and LTFET. The key parameter such as input/output characteristics, capacitance characteristics, GBW, and f_T are analyzed. Benefiting from the no direct overlap between the gate and drain, TGTFET obtains a relatively small C_{gd} and C_{gg}. Finally, TGTFET with remarkable frequency characteristics ($f_T = 11.9$ GHz and GBW = 2.3 GHz) is obtained. As a conclusion, it is expected that TGTFET can be one of the promising alternatives for the next generation of device in low-power and analog/RF applications.

Authors' Contributions

SC puts forward the innovative results in this manuscript and completed the work of simulation and article writing. HL and SW supported the completion of this work and helped in the format modification and detail discussion. WL, XW, and LZ participated in the format modification and detail discussion. All authors read and approved the final manuscript.

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Competing Interests

The authors declare that they have no competing interests.

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References

1. Ionescu AM, Riel H (2011) Tunnel field-effect transistors as energy-efficient electronic switches. Nature. https://doi.org/10.1038/nature10679
2. V. Vijayvargiya and S. K. Vishvakarma. Effect of drain doping profile on double-gate tunnel field-effect transistor and its influence on device RF performance. IEEE Transactions on Nanotechnology. 2014; doi: https://doi.org/10.1109/TNANO.2014.2336812
3. D. Kim, Y. Lee and J. Cai et al. Low power circuit design based on heterojunction tunneling transistors (HETTs). IEEE ISLPED 2009; doi: https://doi.org/10.1109/TVLSI.2012.2213103
4. Hiblot G. et al. Accurate boundary condition for short-channel effect compact modeling in MOS devices. IEEE Transactions on Electron Devices 2015; doi: https://doi.org/10.1109/TED.2014.2368395
5. S. Bangsaruntip, G. M. Cohen, A. Majumdar et al. Universality of short-channel effects in undoped-body silicon nanowire MOSFETs. IEEE Electron Device Lett 2010; doi: https://doi.org/10.1109/LED.2010.2052231
6. J. Madan and R. Chaujar. Gate drain underlapped-PNIN-GAA-TFET for comprehensively upgraded analog/RF performance superlattices and microstructures 2017; doi: https://doi.org/10.1016/j.spmi.2016.12.034
7. G. Singh, S. I. Amin and S. Anand et al. Design of Si 0.5 Ge 0.5 based tunnel field effect transistor and its performance evaluation. Superlattices & Microstructures. 2016; doi: https://doi.org/10.1016/j.spmi.2016.02.027
8. Q. Huang, R. Huang and Z. Zhan et al. A novel Si tunnel FET with 36mV/dec subthreshold slope based on junction depleted-modulation through striped gate configuration. IEEE IEDM 2012; doi: https://doi.org/10.1109/IEDM.2012.6479005
9. U. E. Avci and I. A. Young. Heterojunction TFET scaling and resonant-TFET for steep subthreshold slope at sub-9nm gate-length. IEEE IEDM. 2013; doi: https://doi.org/10.1109/IEDM.2013.6724559
10. W. Y. Choi, B. G. Park and J. D. Lee et al. Tunneling field-effect transistors (TFETs) with subthreshold swing (SS) less than 60 mV/dec. IEEE Electron Device Lett. 2007; doi: https://doi.org/10.1109/LED.2007.901273
11. Appenzeller J., Lin Y. M., Knoch J. et al. Comparing carbon nanotube transistors - the ideal choice: a novel tunneling device design. IEEE Trans. Electron Devices. 2005; doi: https://doi.org/10.1109/TED.2005.859654
12. A. Villalon, G. L. Carval and S. Martinie et al. Further insights in TFET operation. IEEE Trans. Electron Devices. 2014; doi: https://doi.org/10.1109/TED.2014.2325600
13. V. Nagavarapu, R. Jhaveri and J. C. S. Woo. The tunnel source (PNPN) n-MOSFET: a novel high performance transistor. IEEE Trans. Electron Devices. 2008; doi: https://doi.org/10.1109/TED.2008.916711
14. N. Gupta, A. Makosiej and C. Anghel et al. Ultra-low-power compact TFET flip-flop design for high-performance low-voltage applications IEEE ISQED 2016; doi: https://doi.org/10.1109/ISQED.2016.7479184
15. N. Gupta, A. Makosiej and A. Vladimirescu et al. 3T-TFET bitcell based TFET-CMOS hybrid SRAM design for ultra-low power applications. DATE .2016; doi: https://doi.org/10.3850/9783981537079_0462

16. Chen S, Wang S, Liu H, et al. Symmetric U-shaped gate tunnel field-effect transistor. IEEE Transactions on Electron Devices. 2017; doi: https://doi.org/10.1109/TED.2017.2647809
17. Chen S, Liu H, Wang S, et al. Analog/RF performance of two tunnel FETs with symmetric structures. Superlattices & Microstructures 2017; doi: https://doi.org/10.1016/j.spmi.2017.07.013
18. Li W, Liu H, Wang S, et al. Reduced miller capacitance in U-shaped channel tunneling FET by introducing heterogeneous gate dielectric. IEEE Electron Device Lett 2017; doi: https://doi.org/10.1109/LED.2017.2661318
19. Wang Q, Wang S, Liu H et al (2017) Analog/RF performance of L- and U-shaped channel tunneling field-effect transistors and their application as digital inverters. Jpn J Appl Phys. https://doi.org/10.7567/JJAP.56.064102
20. D. B. Abdi and M. J. Kumar. In-built N+ pocket p-n-p-n tunnel field-effect transistor. IEEE Electron Device Lett. 2014; doi: https://doi.org/10.1109/LED.2014.2362926
21. W. Cao, C. J. Yao and G. F. Jiao et al. Improvement in reliability of tunneling field-effect transistor with p-n-i-n structure. IEEE Trans. Electron Devices. 2011; doi: https://doi.org/10.1109/TED.2011.2144987
22. A. Mallik, A. Chattopadhyay and S. Guin et al. Impact of a spacer–drain overlap on the characteristics of a silicon tunnel field-effect transistor based on vertical tunneling. IEEE Trans Electron Devices 2013; doi: https://doi.org/10.1109/TED.2013.2237776
23. Kim SW, Choi WY, Sun MC et al (2012) Design guideline of Si-based L-shaped tunneling field-effect transistors. Jpn J Appl Phys. https://doi.org/10.1143/JJAP.51.06FE09
24. S. W. Kim, J. H. Kim and T. J. K. Liu et al. Demonstration of L-shaped tunnel field-effect transistors. IEEE Trans. Electron Devices. 2016; doi: https://doi.org/10.1109/TED.2015.2472496
25. W. Wang, P. F. Wang and C. M. Zhang et al. Design of U-shape channel tunnel FETs with SiGe source regions. IEEE Trans. Electron Devices. 2014; doi: https://doi.org/10.1109/TED.2013.2289075
26. Y. Morita, T. Mori and S. Migita et al. Performance enhancement of tunnel field-effect transistors by synthetic electric field effect, IEEE Electron Device Lett. 2014; doi: https://doi.org/10.1109/LED.2014.2323337
27. Boucart K, Ionescu AM (2007) Length scaling of the double gate tunnel FET with a high-k gate dielectric. Solid State Electron. https://doi.org/10.1016/j.sse.2007.09.014
28. Narang R, Saxena M, GuptaR S, et al. Linearity and analog performance analysis of double gate tunnel FET: effect of temperature and gate stack. International Journal of VLSI Design & Communication Systems (VLSICS) 2011; doi: https://doi.org/10.1007/978-3-642-22543-7_47
29. Gupta S K, Baishya S. Analog and RF performance evaluation of dual metal double gate high-k stack (DMDG-HKS) MOSFETs. J Nano Electron Phys. 2013; Available: https://jnep.sumdu.edu.ua/en/component/ search/index.php?option=com_content&task=full_article&id=984
30. Akram M. W., B. Ghosh. Analog performance of double gate junctionless tunnel field effect transistor. Journal of Semiconductors. 2014; doi: https://doi.org/10.1088/1674-4926/35/7/074001
31. Mohankumar N, Syamal B, Sarkar CK (2009) Investigation of novel attributes of single halo dual-material double gate MOSFETs for analog/RF applications. Microelectron Rel. https://doi.org/10.1016/j.microrel.2009.06.006